

- **Very Low Power Consumption**  
– 1 mW Typ at  $V_{DD} = 5\text{ V}$
- **Capable of Operation in Astable Mode**
- **CMOS Output Capable of Swinging Rail to Rail**
- **High Output-Current Capability**  
– Sink 100 mA Typ  
– Source 10 mA Typ
- **Output Fully Compatible With CMOS, TTL, and MOS**
- **Low Supply Current Reduces Spikes During Output Transitions**
- **Single-Supply Operation From 2 V to 15 V**
- **Functionally Interchangeable With the NE555; Has Same Pinout**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015.2**
- **Available in Q-Temp Automotive High Reliability Automotive Applications Configuration Control/Print Support Qualification to Automotive Standards**

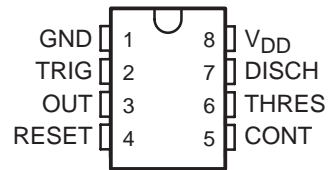
## description

The TLC555 is a monolithic timing circuit fabricated using the TI LinCMOS™ process. The timer is fully compatible with CMOS, TTL, and MOS logic and operates at frequencies up to 2 MHz. Because of its high input impedance, this device uses smaller timing capacitors than those used by the NE555. As a result, more accurate time delays and oscillations are possible. Power consumption is low across the full range of power supply voltage.

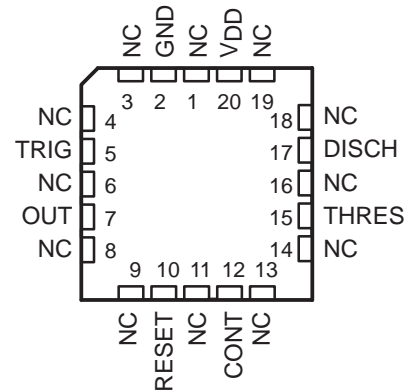
Like the NE555, the TLC555 has a trigger level equal to approximately one-third of the supply voltage and a threshold level equal to approximately two-thirds of the supply voltage. These levels can be altered by use of the control voltage terminal (CONT). When the trigger input (TRIG) falls below the trigger level, the flip-flop is set and the output goes high. If TRIG is above the trigger level and the threshold input (THRES) is above the threshold level, the flip-flop is reset and the output is low. The reset input (RESET) can override all other inputs and can be used to initiate a new timing cycle. If RESET is low, the flip-flop is reset and the output is low. Whenever the output is low, a low-impedance path is provided between the discharge terminal (DISCH) and GND. All unused inputs should be tied to an appropriate logic level to prevent false triggering.

While the CMOS output is capable of sinking over 100 mA and sourcing over 10 mA, the TLC555 exhibits greatly reduced supply-current spikes during output transitions. This minimizes the need for the large decoupling capacitors required by the NE555.

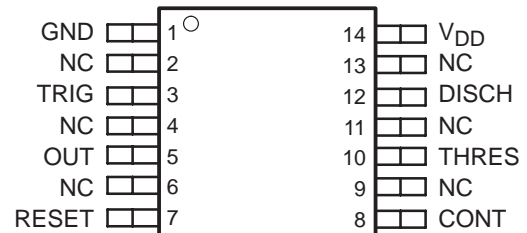
**D, DB, JG, OR P PACKAGE  
(TOP VIEW)**



**FK PACKAGE  
(TOP VIEW)**



**PW PACKAGE  
(TOP VIEW)**



NC – No internal connection



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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# TLC555 LinCMOS™ TIMER

SLFS043F – SEPTEMBER 1983 – REVISED FEBRUARY 2005

## description (continued)

The TLC555C is characterized for operation from 0°C to 70°C. The TLC555I is characterized for operation from –40°C to 85°C. The TLC555Q is characterized for operation over the automotive temperature range of –40°C to 125°C. The TLC555M is characterized for operation over the full military temperature range of –55°C to 125°C.

### AVAILABLE OPTIONS†

| PACKAGED DEVICES |                       |                    |            |                   |                  |                 |             |
|------------------|-----------------------|--------------------|------------|-------------------|------------------|-----------------|-------------|
| T <sub>A</sub>   | V <sub>DD</sub> RANGE | SMALL OUTLINE (D)‡ | SSOP (DB)‡ | CHIP CARRIER (FK) | CERAMIC DIP (JG) | PLASTIC DIP (P) | TSSOP (PW)‡ |
| 0°C to 70°C      | 2 V to 15 V           | TLC555CD           | TLC555CDB  | —                 | —                | TLC555CP        | TLC555CPW   |
| –40°C to 85°C    | 3 V to 15 V           | TLC555ID           | —          | —                 | —                | TLC555IP        | —           |
| –40°C to 125°C   | 5 V to 15 V           | TLC555QD           | —          | —                 | —                | —               | —           |
| –55°C to 125°C   | 5 V to 15 V           | TLC555MD           | —          | TLC555MFK         | TLC555MJG        | TLC555MP        | —           |

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

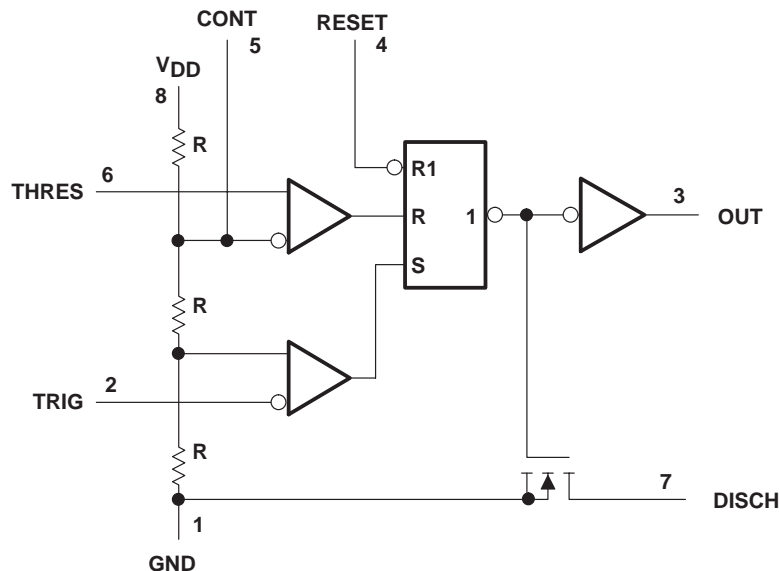
‡ This package is available taped and reeled. Add the R suffix to device type (e.g., TLC555CDR).

### FUNCTION TABLE

| RESET VOLTAGE‡ | TRIGGER VOLTAGE‡ | THRESHOLD VOLTAGE‡ | OUTPUT                    | DISCHARGE SWITCH |
|----------------|------------------|--------------------|---------------------------|------------------|
| <MIN           | Irrelevant       | Irrelevant         | L                         | On               |
| >MAX           | <MIN             | Irrelevant         | H                         | Off              |
| >MAX           | >MAX             | >MAX               | L                         | On               |
| >MAX           | >MAX             | <MIN               | As previously established |                  |

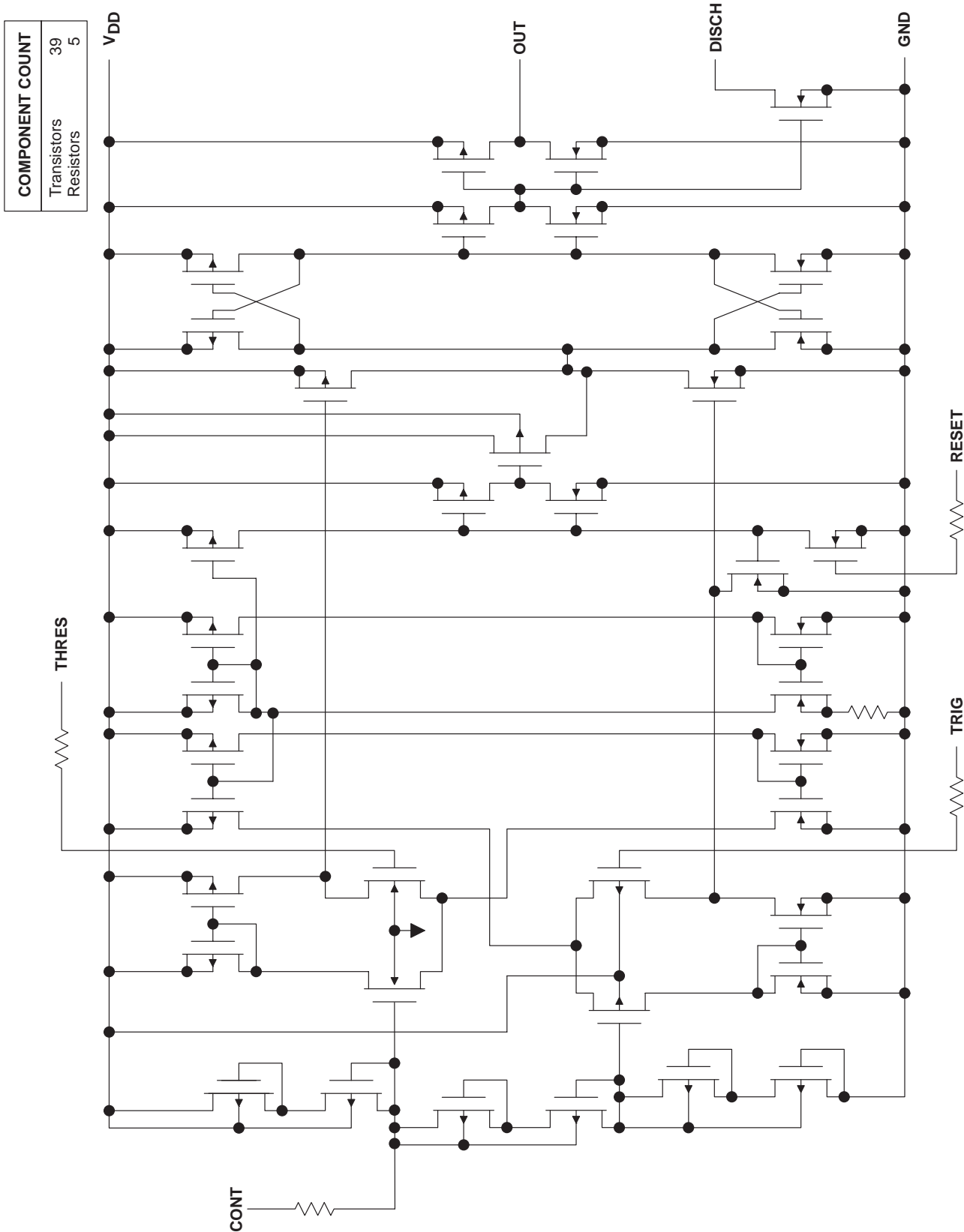
‡ For conditions shown as MIN or MAX, use the appropriate value specified under electrical characteristics.

## functional block diagram



Pin numbers are for all packages except the FK package. RESET can override TRIG, which can override THRES.

equivalent schematic (each channel)



# TLC555 LinCMOS™ TIMER

SLFS043F – SEPTEMBER 1983 – REVISED FEBRUARY 2005

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

|   |                              |
|---|------------------------------|
| Supply voltage, $V_{DD}$ (see Note 1)   | 18 V                         |
| Input voltage range, $V_I$ (any input)  | -0.3 to $V_{DD}$             |
| Sink current, discharge or output   | 150 mA                       |
| Source current, output, $I_O$   | 15 mA                        |
| Continuous total power dissipation  | See Dissipation Rating Table |
| Operating free-air temperature range, $T_A$ :   |                              |
| C-suffix  | 0°C to 70°C                  |
| I-suffix  | -40°C to 85°C                |
| Q-suffix  | -40°C to 125°C               |
| M-suffix  | -55°C to 125°C               |
| Storage temperature range   | -65°C to 150°C               |
| Case temperature for 60 seconds: FK package   | 260°C                        |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package              | 300°C                        |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, DB, P, or PW package | 260°C                        |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network GND.

DISSIPATION RATING TABLE

| PACKAGE | $T_A \leq 25^\circ\text{C}$<br>POWER RATING | DERATING FACTOR<br>ABOVE $T_A = 25^\circ\text{C}$ | $T_A = 70^\circ\text{C}$<br>POWER RATING | $T_A = 85^\circ\text{C}$<br>POWER RATING | $T_A = 125^\circ\text{C}$<br>POWER RATING |
|---------|---|---|--|--|---|
| D       | 725 mW                                      | 5.8 mW/°C   | 464 mW                                   | 377 mW                                   | 145 mW                                    |
| DB      | 525 mW                                      | 4.2 mW/°C   | 336 mW                                   | 273 mW                                   | 105 mW                                    |
| FK      | 1375 mW                                     | 11.0 mW/°C  | 880 mW                                   | 715 mW                                   | 275 mW                                    |
| JG      | 1050 mW                                     | 8.4 mW/°C   | 672 mW                                   | 546 mW                                   | 210 mW                                    |
| P       | 1000 mW                                     | 8.0 mW/°C   | 640 mW                                   | 520 mW                                   | 200 mW                                    |
| PW      | 525 mW                                      | 4.2 mW/°C   | 336 mW                                   | 273 mW                                   | 105 mW                                    |

## recommended operating conditions

|   |         | MIN | MAX | UNIT |
|---|---------|-----|-----|------|
| Supply voltage, $V_{DD}$                    |         | 2   | 15  | V    |
| Operating free-air temperature range, $T_A$ | TLC555C | 0   | 70  | °C   |
|   | TLC555I | -40 | 85  |      |
|   | TLC555Q | -40 | 125 |      |
|   | TLC555M | -55 | 125 |      |



**electrical characteristics at specified free-air temperature,  $V_{DD} = 2\text{ V}$  for TLC555C,  $V_{DD} = 3\text{ V}$  for TLC555I**

| PARAMETER  | TEST CONDITIONS                    | $T_A$ †    | TLC555C |      |      | TLC555I |      |      | UNIT          |
|--|------------------------------------|------------|---------|------|------|---------|------|------|---------------|
|  |                                    |            | MIN     | TYP  | MAX  | MIN     | TYP  | MAX  |               |
| $V_{IT}$ Threshold voltage                                       |                                    | 25°C       | 0.95    | 1.33 | 1.65 | 1.6     |      | 2.4  | V             |
|  |                                    | Full range | 0.85    |      | 1.75 | 1.5     |      | 2.5  |               |
| $I_{IT}$ Threshold current                                       |                                    | 25°C       | 10      |      |      | 10      |      |      | pA            |
|  |                                    | MAX        | 75      |      |      | 150     |      |      |               |
| $V_{I(TRIG)}$ Trigger voltage                                    |                                    | 25°C       | 0.4     | 0.67 | 0.95 | 0.71    | 1    | 1.29 | V             |
|  |                                    | Full range | 0.3     |      | 1.05 | 0.61    |      | 1.39 |               |
| $I_{I(TRIG)}$ Trigger current                                    |                                    | 25°C       | 10      |      |      | 10      |      |      | pA            |
|  |                                    | MAX        | 75      |      |      | 150     |      |      |               |
| $V_{I(RESET)}$ Reset voltage                                     |                                    | 25°C       | 0.4     | 1.1  | 1.5  | 0.4     | 1.1  | 1.5  | V             |
|  |                                    | Full range | 0.3     |      | 2    | 0.3     |      | 1.8  |               |
| $I_{I(RESET)}$ Reset current                                     |                                    | 25°C       | 10      |      |      | 10      |      |      | pA            |
|  |                                    | MAX        | 75      |      |      | 150     |      |      |               |
| Control voltage (open circuit) as a percentage of supply voltage |                                    | MAX        | 66.7%   |      |      | 66.7%   |      |      |               |
| Discharge switch on-stage voltage                                | $I_{OL} = 1\text{ mA}$             | 25°C       | 0.03    |      |      | 0.03    |      |      | V             |
|  |                                    | Full range | 0.2     |      |      | 0.25    |      |      |               |
| Discharge switch off-stage current                               |                                    | 25°C       | 0.1     |      |      | 0.1     |      |      | nA            |
|  |                                    | MAX        | 0.5     |      |      | 120     |      |      |               |
| $V_{OH}$ High-level output voltage                               | $I_{OH} = -300\text{ }\mu\text{A}$ | 25°C       | 1.5     | 1.9  |      | 2.5     | 2.85 |      | V             |
|  |                                    | Full range | 1.5     |      |      | 2.5     |      |      |               |
| $V_{OL}$ Low-level output voltage                                | $I_{OL} = 1\text{ mA}$             | 25°C       | 0.07    |      |      | 0.07    |      |      | V             |
|  |                                    | Full range | 0.3     |      |      | 0.35    |      |      |               |
| $I_{DD}$ Supply current  | See Note 2                         | 25°C       | 250     |      |      | 250     |      |      | $\mu\text{A}$ |
|  |                                    | Full range | 400     |      |      | 500     |      |      |               |

† Full range is 0°C to 70°C for the TLC555C and -40°C to 85°C for the TLC555I. For conditions shown as MAX, use the appropriate value specified in the recommended operating conditions table.

NOTE 2: These values apply for the expected operating configurations in which THRES is connected directly to DISCH or to TRIG.

# TLC555 LinCMOS™ TIMER

SLFS043F – SEPTEMBER 1983 – REVISED FEBRUARY 2005

## electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

| PARAMETER  | TEST CONDITIONS          | $T_A$ †    | TLC555C |      |      | TLC555I |      |      | TLC555Q, TLC555M |      |      | UNIT          |
|--|--------------------------|------------|---------|------|------|---------|------|------|------------------|------|------|---------------|
|  |                          |            | MIN     | TYP  | MAX  | MIN     | TYP  | MAX  | MIN              | TYP  | MAX  |               |
| $V_{IT}$ Threshold voltage                                       |                          | 25°C       | 2.8     | 3.3  | 3.8  | 2.8     | 3.3  | 3.8  | 2.8              | 3.3  | 3.8  | V             |
|  |                          | Full range | 2.7     |      | 3.9  | 2.7     |      | 3.9  | 2.7              |      | 3.9  |               |
| $I_{IT}$ Threshold current                                       |                          | 25°C       | 10      |      |      | 10      |      |      | 10               |      |      | pA            |
|  |                          | MAX        | 75      |      |      | 150     |      |      | 5000             |      |      |               |
| $V_{I(TRIG)}$ Trigger voltage                                    |                          | 25°C       | 1.36    | 1.66 | 1.96 | 1.36    | 1.66 | 1.96 | 1.36             | 1.66 | 1.96 | V             |
|  |                          | Full range | 1.26    |      | 2.06 | 1.26    |      | 2.06 | 1.26             |      | 2.06 |               |
| $I_{I(TRIG)}$ Trigger current                                    |                          | 25°C       | 10      |      |      | 10      |      |      | 10               |      |      | pA            |
|  |                          | MAX        | 75      |      |      | 150     |      |      | 5000             |      |      |               |
| $V_{I(RESET)}$ Reset voltage                                     |                          | 25°C       | 0.4     | 1.1  | 1.5  | 0.4     | 1.1  | 1.5  | 0.4              | 1.1  | 1.5  | V             |
|  |                          | Full range | 0.3     |      | 1.8  | 0.3     |      | 1.8  | 0.3              |      | 1.8  |               |
| $I_{I(RESET)}$ Reset current                                     |                          | 25°C       | 10      |      |      | 10      |      |      | 10               |      |      | pA            |
|  |                          | MAX        | 75      |      |      | 150     |      |      | 5000             |      |      |               |
| Control voltage (open circuit) as a percentage of supply voltage |                          | MAX        | 66.7%   |      |      | 66.7%   |      |      | 66.7%            |      |      |               |
| Discharge switch on-state voltage                                | $I_{OL} = 10\text{ mA}$  | 25°C       | 0.14    |      |      | 0.14    |      |      | 0.14             |      |      | V             |
|  |                          | Full range | 0.6     |      |      | 0.6     |      |      | 0.6              |      |      |               |
| Discharge switch off-state current                               |                          | 25°C       | 0.1     |      |      | 0.1     |      |      | 0.1              |      |      | nA            |
|  |                          | MAX        | 0.5     |      |      | 120     |      |      | 120              |      |      |               |
| $V_{OH}$ High-level output voltage                               | $I_{OH} = -1\text{ mA}$  | 25°C       | 4.1     | 4.8  |      | 4.1     | 4.8  |      | 4.1              | 4.8  |      | V             |
|  |                          | Full range | 4.1     |      |      | 4.1     |      |      | 4.1              |      |      |               |
| $V_{OL}$ Low-level output voltage                                | $I_{OL} = 8\text{ mA}$   | 25°C       | 0.21    |      |      | 0.21    |      |      | 0.21             |      |      | V             |
|  |                          | Full range | 0.5     |      |      | 0.5     |      |      | 0.6              |      |      |               |
|  | $I_{OL} = 5\text{ mA}$   | 25°C       | 0.13    |      |      | 0.13    |      |      | 0.13             |      |      |               |
|  |                          | Full range | 0.4     |      |      | 0.4     |      |      | 0.45             |      |      |               |
|  | $I_{OL} = 3.2\text{ mA}$ | 25°C       | 0.08    |      |      | 0.08    |      |      | 0.08             |      |      |               |
|  |                          | Full range | 0.35    |      |      | 0.35    |      |      | 0.4              |      |      |               |
| $I_{DD}$ Supply current  | See Note 2               | 25°C       | 170     | 350  |      | 170     | 350  |      | 170              | 350  |      | $\mu\text{A}$ |
|  |                          | Full range | 500     |      |      | 600     |      |      | 700              |      |      |               |

† Full range is 0°C to 70°C the for TLC555C, -40°C to 85°C for the TLC555I, -40°C to 125°C for the TLC555Q, and -55°C to 125°C for the TLC555M. For conditions shown as MAX, use the appropriate value specified in the recommended operating conditions table.

NOTE 2: These values apply for the expected operating configurations in which THRES is connected directly to DISCH or TRIG.



**electrical characteristics at specified free-air temperature,  $V_{DD} = 15\text{ V}$**

| PARAMETER  | TEST CONDITIONS          | $T_A$ †    | TLC555C |      |       | TLC555I |      |       | TLC555Q, TLC555M |      |       | UNIT |
|--|--------------------------|------------|---------|------|-------|---------|------|-------|------------------|------|-------|------|
|  |                          |            | MIN     | TYP  | MAX   | MIN     | TYP  | MAX   | MIN              | TYP  | MAX   |      |
| $V_{IT}$ Threshold voltage                                       |                          | 25°C       | 9.45    | 10   | 10.55 | 9.45    | 10   | 10.55 | 9.45             | 10   | 10.55 | V    |
|  |                          | Full range | 9.35    |      | 10.65 | 9.35    |      | 10.65 | 9.35             |      | 10.65 |      |
| $I_{IT}$ Threshold current                                       |                          | 25°C       |         | 10   |       |         | 10   |       |                  | 10   |       | pA   |
|  |                          | MAX        |         | 75   |       |         | 150  |       |                  | 5000 |       |      |
| $V_{I(TRIG)}$ Trigger voltage                                    |                          | 25°C       | 4.65    | 5    | 5.35  | 4.65    | 5    | 5.35  | 4.65             | 5    | 5.35  | V    |
|  |                          | Full range | 4.55    |      | 5.45  | 4.55    |      | 5.45  | 4.55             |      | 5.45  |      |
| $I_{I(TRIG)}$ Trigger current                                    |                          | 25°C       |         | 10   |       |         | 10   |       |                  | 10   |       | pA   |
|  |                          | MAX        |         | 75   |       |         | 150  |       |                  | 5000 |       |      |
| $V_{I(RESET)}$ Reset voltage                                     |                          | 25°C       | 0.4     | 1.1  | 1.5   | 0.4     | 1.1  | 1.5   | 0.4              | 1.1  | 1.5   | V    |
|  |                          | Full range | 0.3     |      | 1.8   | 0.3     |      | 1.8   | 0.3              |      | 1.8   |      |
| $I_{I(RESET)}$ Reset current                                     |                          | 25°C       |         | 10   |       |         | 10   |       |                  | 10   |       | pA   |
|  |                          | MAX        |         | 75   |       |         | 150  |       |                  | 5000 |       |      |
| Control voltage (open circuit) as a percentage of supply voltage |                          | MAX        | 66.7%   |      |       | 66.7%   |      |       | 66.7%            |      |       |      |
| Discharge switch on-state voltage                                | $I_{OL} = 100\text{ mA}$ | 25°C       |         | 0.77 | 1.7   |         | 0.77 | 1.7   |                  | 0.77 | 1.7   | V    |
|  |                          | Full range |         |      | 1.8   |         |      | 1.8   |                  |      | 1.8   |      |
| Discharge switch off-state current                               |                          | 25°C       |         | 0.1  |       |         | 0.1  |       |                  | 0.1  |       | nA   |
|  |                          | MAX        |         | 0.5  |       |         | 120  |       |                  | 120  |       |      |
| $V_{OH}$ High-level output voltage                               | $I_{OH} = -10\text{ mA}$ | 25°C       | 12.5    | 14.2 |       | 12.5    | 14.2 |       | 12.5             | 14.2 |       | V    |
|  |                          | Full range | 12.5    |      |       | 12.5    |      |       | 12.5             |      |       |      |
|  | $I_{OH} = -5\text{ mA}$  | 25°C       | 13.5    | 14.6 |       | 13.5    | 14.6 |       | 13.5             | 14.6 |       |      |
|  |                          | Full range | 13.5    |      |       | 13.5    |      |       | 13.5             |      |       |      |
|  | $I_{OH} = -1\text{ mA}$  | 25°C       | 14.2    | 14.9 |       | 14.2    | 14.9 |       | 14.2             | 14.9 |       |      |
|  |                          | Full range | 14.2    |      |       | 14.2    |      |       | 14.2             |      |       |      |
| $V_{OL}$ Low-level output voltage                                | $I_{OL} = 100\text{ mA}$ | 25°C       |         | 1.28 | 3.2   |         | 1.28 | 3.2   |                  | 1.28 | 3.2   | V    |
|  |                          | Full range |         |      | 3.6   |         |      | 3.7   |                  |      | 3.8   |      |
|  | $I_{OL} = 50\text{ mA}$  | 25°C       |         | 0.63 | 1     |         | 0.63 | 1     |                  | 0.63 | 1     |      |
|  |                          | Full range |         |      | 1.3   |         |      | 1.4   |                  |      | 1.5   |      |
|  | $I_{OL} = 10\text{ mA}$  | 25°C       |         | 0.12 | 0.3   |         | 0.12 | 0.3   |                  | 0.12 | 0.3   |      |
|  |                          | Full range |         |      | 0.4   |         |      | 0.4   |                  |      | 0.45  |      |
| $I_{DD}$ Supply current  | See Note 2               | 25°C       |         | 360  | 600   |         | 360  | 600   |                  | 360  | 600   | μA   |
|  |                          | Full range |         |      | 800   |         |      | 900   |                  |      | 1000  |      |

† Full range is 0°C to 70°C for TLC555C, -40°C to 85°C for TLC555I, -40°C to 125°C for the TLC555Q, and -55°C to 125°C for TLC555M. For conditions shown as MAX, use the appropriate value specified in the recommended operating conditions table.

NOTE 2: These values apply for the expected operating configurations in which THRES is connected directly to DISCH or TRIG.

# TLC555 LinCMOS™ TIMER

SLFS043F – SEPTEMBER 1983 – REVISED FEBRUARY 2005

## operating characteristics, $V_{DD} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$ (unless otherwise noted)

| PARAMETER                                     | TEST CONDITIONS  | MIN | TYP | MAX | UNIT |
|---|--|-----|-----|-----|------|
| Initial error of timing interval‡             | $V_{DD} = 5\text{ V to }15\text{ V}$ , $R_A = R_B = 1\text{ k}\Omega\text{ to }100\text{ k}\Omega$ ,<br>$C_T = 0.1\text{ }\mu\text{F}$ ,<br>See Note 3 |     | 1%  | 3%  |      |
| Supply voltage sensitivity of timing interval |  |     | 0.1 | 0.5 | %/V  |
| $t_r$ Output pulse rise time                  | $R_L = 10\text{ M}\Omega$ , $C_L = 10\text{ pF}$   |     | 20  | 75  | ns   |
| $t_f$ Output pulse fall time                  |  |     | 15  | 60  |      |
| $f_{max}$ Maximum frequency in astable mode   | $R_A = 470\text{ }\Omega$ ,<br>$C_T = 200\text{ pF}$ , $R_B = 200\text{ }\Omega$ ,<br>See Note 3   | 1.2 | 2.1 |     | MHz  |

‡ Timing interval error is defined as the difference between the measured value and the average value of a random sample from each process run.

NOTE 3:  $R_A$ ,  $R_B$ , and  $C_T$  are as defined in Figure 1.

## electrical characteristics at $V_{DD} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$

| PARAMETER  | TEST CONDITIONS          | MIN  | TYP   | MAX  | UNIT          |
|--|--------------------------|------|-------|------|---------------|
| $V_{IT}$ Threshold voltage                                       |                          | 2.8  | 3.3   | 3.8  | V             |
| $I_{IT}$ Threshold current                                       |                          |      | 10    |      | pA            |
| $V_{I(TRIG)}$ Trigger voltage                                    |                          | 1.36 | 1.66  | 1.96 | V             |
| $I_{I(TRIG)}$ Trigger current                                    |                          |      | 10    |      | pA            |
| $V_{I(RESET)}$ Reset voltage                                     |                          | 0.4  | 1.1   | 1.5  | V             |
| $I_{I(RESET)}$ Reset current                                     |                          |      | 10    |      | pA            |
| Control voltage (open circuit) as a percentage of supply voltage |                          |      | 66.7% |      |               |
| Discharge switch on-state voltage                                | $I_{OL} = 10\text{ mA}$  |      | 0.14  | 0.5  | V             |
| Discharge switch off-state current                               |                          |      | 0.1   |      | nA            |
| $V_{OH}$ High-level output voltage                               | $I_{OH} = -1\text{ mA}$  | 4.1  | 4.8   |      | V             |
| $V_{OL}$ Low-level output voltage                                | $I_{OL} = 8\text{ mA}$   |      | 0.21  | 0.4  | V             |
|  | $I_{OL} = 5\text{ mA}$   |      | 0.13  | 0.3  |               |
|  | $I_{OL} = 3.2\text{ mA}$ |      | 0.08  | 0.3  |               |
| $I_{DD}$ Supply current  | See Note 2               |      | 170   | 350  | $\mu\text{A}$ |

NOTE 2: These values apply for the expected operating configurations in which THRES is connected directly to DISCH or TRIG.



TYPICAL CHARACTERISTICS

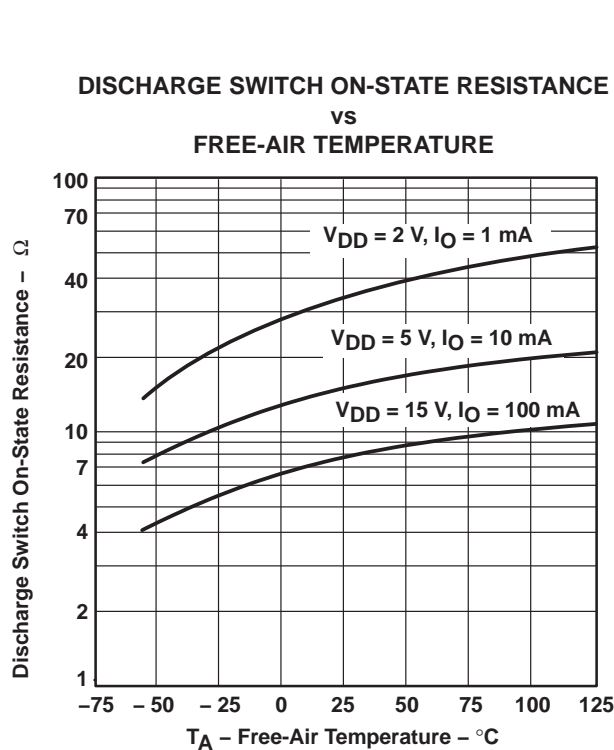
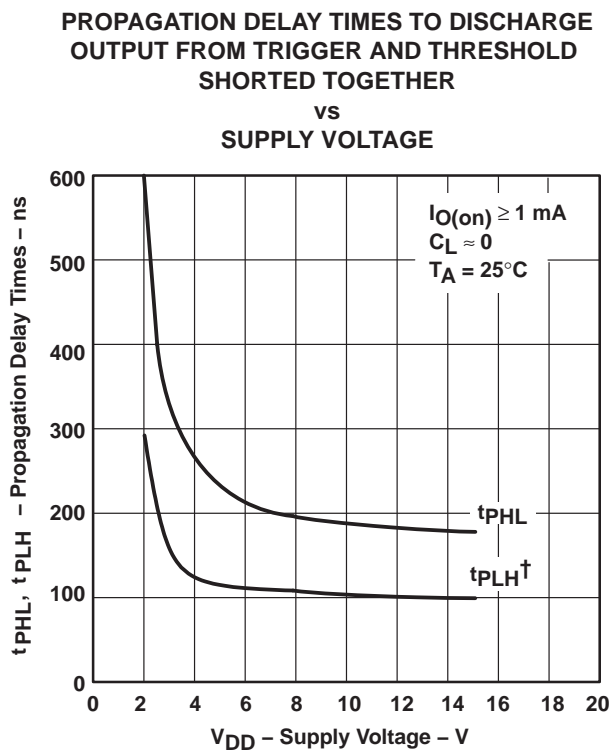


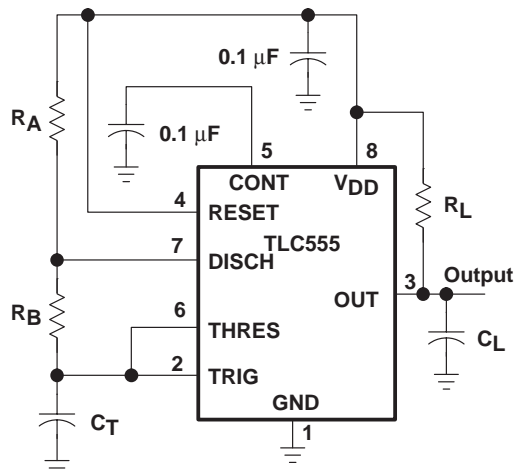
Figure 1



† The effects of the load resistance on these values must be taken into account separately.

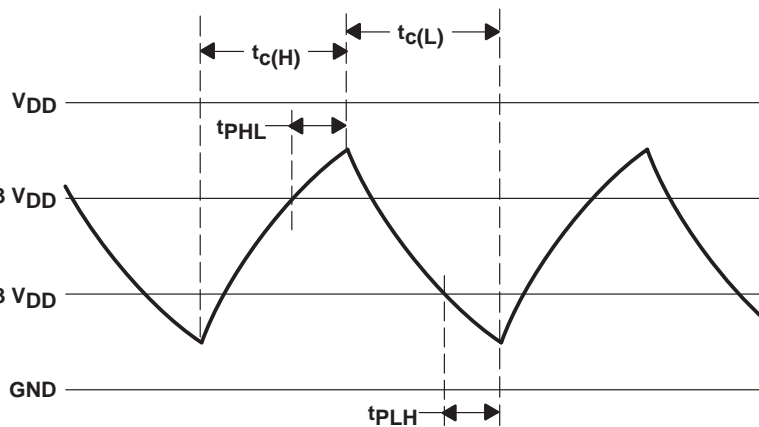
Figure 2

APPLICATION INFORMATION



Pin numbers shown are for all packages except the FK package.

CIRCUIT



TRIGGER AND THRESHOLD VOLTAGE WAVEFORM

Figure 3. Astable Operation

**APPLICATION INFORMATION**

Connecting TRIG to THRES, as shown in Figure 3, causes the timer to run as a multivibrator. The capacitor  $C_T$  charges through  $R_A$  and  $R_B$  to the threshold voltage level (approximately  $0.67 V_{DD}$ ) and then discharges through  $R_B$  only to the value of the trigger voltage level (approximately  $0.33 V_{DD}$ ). The output is high during the charging cycle ( $t_{c(H)}$ ) and low during the discharge cycle ( $t_{c(L)}$ ). The duty cycle is controlled by the values of  $R_A$ ,  $R_B$ , and  $C_T$  as shown in the equations below.

$$t_{c(H)} \approx C_T (R_A + R_B) \ln 2 \quad (\ln 2 = 0.693)$$

$$t_{c(L)} \approx C_T R_B \ln 2$$

$$\text{Period} = t_{c(H)} + t_{c(L)} \approx C_T (R_A + 2R_B) \ln 2$$

$$\text{Output driver duty cycle} = \frac{t_{c(L)}}{t_{c(H)} + t_{c(L)}} \approx 1 - \frac{R_B}{R_A + 2R_B}$$

$$\text{Output waveform duty cycle} = \frac{t_{c(H)}}{t_{c(H)} + t_{c(L)}} \approx \frac{R_B}{R_A + 2R_B}$$

The 0.1- $\mu$ F capacitor at CONT in Figure 3 decreases the period by about 10%.

The formulas shown above do not allow for any propagation delay times from the TRIG and THRES inputs to DISCH. These delay times add directly to the period and create differences between calculated and actual values that increase with frequency. In addition, the internal on-state resistance  $r_{on}$  during discharge adds to  $R_B$  to provide another source of timing error in the calculation when  $R_B$  is very low or  $r_{on}$  is very high.

The equations below provide better agreement with measured values.

$$t_{c(H)} = C_T (R_A + R_B) \ln \left[ 3 - \exp \left( \frac{-t_{PLH}}{C_T (R_B + r_{on})} \right) \right] + t_{PHL}$$

$$t_{c(L)} = C_T (R_B + r_{on}) \ln \left[ 3 - \exp \left( \frac{-t_{PHL}}{C_T (R_A + R_B)} \right) \right] + t_{PLH}$$

These equations and those given earlier are similar in that a time constant is multiplied by the logarithm of a number or function. The limit values of the logarithmic terms must be between  $\ln 2$  at low frequencies and  $\ln 3$  at extremely high frequencies. For a duty cycle close to 50%, an appropriate constant for the logarithmic terms can be substituted

with good results. Duty cycles less than 50%  $\frac{t_{c(H)}}{t_{c(H)} + t_{c(L)}}$  require that  $\frac{t_{c(H)}}{t_{c(L)}} < 1$  and possibly  $R_A \leq r_{on}$ . These

conditions can be difficult to obtain.

In monostable applications, the trip point on TRIG can be set by a voltage applied to CONT. An input voltage between 10% and 80% of the supply voltage from a resistor divider with at least 500- $\mu$ A bias provides good results.

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/<br>Ball Finish | MSL Peak Temp <sup>(3)</sup> | Samples<br>(Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|----------------------|------------------------------|-----------------------------|
| 5962-89503012A   | ACTIVE                | LCCC         | FK              | 20   | 1           | TBD                     | Call TI              | Call TI                      |                             |
| 5962-8950301PA   | ACTIVE                | CDIP         | JG              | 8    | 1           | TBD                     | Call TI              | Call TI                      |                             |
| TLC555CD         | ACTIVE                | SOIC         | D               | 8    | 75          | Green (RoHS & no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| TLC555CDG4       | ACTIVE                | SOIC         | D               | 8    | 75          | Green (RoHS & no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| TLC555CDR        | ACTIVE                | SOIC         | D               | 8    | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| TLC555CDRG4      | ACTIVE                | SOIC         | D               | 8    | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| TLC555CP         | ACTIVE                | PDIP         | P               | 8    | 50          | Pb-Free (RoHS)          | CU NIPDAU            | N / A for Pkg Type           |                             |
| TLC555CPE4       | ACTIVE                | PDIP         | P               | 8    | 50          | Pb-Free (RoHS)          | CU NIPDAU            | N / A for Pkg Type           |                             |
| TLC555CPSR       | ACTIVE                | SO           | PS              | 8    | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| TLC555CPSRG4     | ACTIVE                | SO           | PS              | 8    | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| TLC555CPW        | ACTIVE                | TSSOP        | PW              | 14   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| TLC555CPWG4      | ACTIVE                | TSSOP        | PW              | 14   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| TLC555CPWR       | ACTIVE                | TSSOP        | PW              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| TLC555CPWRG4     | ACTIVE                | TSSOP        | PW              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| TLC555ID         | ACTIVE                | SOIC         | D               | 8    | 75          | Green (RoHS & no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| TLC555IDG4       | ACTIVE                | SOIC         | D               | 8    | 75          | Green (RoHS & no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| TLC555IDR        | ACTIVE                | SOIC         | D               | 8    | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| TLC555IDRG4      | ACTIVE                | SOIC         | D               | 8    | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| TLC555IP         | ACTIVE                | PDIP         | P               | 8    | 50          | Pb-Free (RoHS)          | CU NIPDAU            | N / A for Pkg Type           |                             |

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup>    | Lead/<br>Ball Finish | MSL Peak Temp <sup>(3)</sup> | Samples<br>(Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|----------------------------|----------------------|------------------------------|-----------------------------|
| TLC555IPE4       | ACTIVE                | PDIP         | P               | 8    | 50          | Pb-Free (RoHS)             | CU NIPDAU            | N / A for Pkg Type           |                             |
| TLC555MFKB       | ACTIVE                | LCCC         | FK              | 20   | 1           | TBD                        | POST-PLATE           | N / A for Pkg Type           |                             |
| TLC555MJG        | ACTIVE                | CDIP         | JG              | 8    | 1           | TBD                        | A42                  | N / A for Pkg Type           |                             |
| TLC555MJGB       | ACTIVE                | CDIP         | JG              | 8    | 1           | TBD                        | A42                  | N / A for Pkg Type           |                             |
| TLC555MP         | OBSOLETE              | PDIP         | P               | 8    |             | TBD                        | Call TI              | Call TI                      |                             |
| TLC555QDR        | ACTIVE                | SOIC         | D               | 8    | 2500        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| TLC555QDRG4      | ACTIVE                | SOIC         | D               | 8    | 2500        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**OTHER QUALIFIED VERSIONS OF TLC555, TLC555M :**

- Catalog: [TLC555](#)
- Automotive: [TLC555-Q1](#), [TLC555-Q1](#)
- Military: [TLC555M](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


|    |   |
|----|---|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TLC555CDR  | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| TLC555CPSR | SO           | PS              | 8    | 2000 | 330.0              | 16.4               | 8.2     | 6.6     | 2.5     | 12.0    | 16.0   | Q1            |
| TLC555CPWR | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| TLC555IDR  | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| TLC555QDR  | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TLC555CDR  | SOIC         | D               | 8    | 2500 | 340.5       | 338.1      | 20.6        |
| TLC555CPSR | SO           | PS              | 8    | 2000 | 367.0       | 367.0      | 38.0        |
| TLC555CPWR | TSSOP        | PW              | 14   | 2000 | 367.0       | 367.0      | 35.0        |
| TLC555IDR  | SOIC         | D               | 8    | 2500 | 340.5       | 338.1      | 20.6        |
| TLC555QDR  | SOIC         | D               | 8    | 2500 | 367.0       | 367.0      | 35.0        |

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification.  
 E. Falls within MIL STD 1835 GDIP1-T8



FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A                |                  | B                |                  |
|---------------------|------------------|------------------|------------------|------------------|
|                     | MIN              | MAX              | MIN              | MAX              |
| 20                  | 0.342<br>(8,69)  | 0.358<br>(9,09)  | 0.307<br>(7,80)  | 0.358<br>(9,09)  |
| 28                  | 0.442<br>(11,23) | 0.458<br>(11,63) | 0.406<br>(10,31) | 0.458<br>(11,63) |
| 44                  | 0.640<br>(16,26) | 0.660<br>(16,76) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 52                  | 0.740<br>(18,78) | 0.761<br>(19,32) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 68                  | 0.938<br>(23,83) | 0.962<br>(24,43) | 0.850<br>(21,6)  | 0.858<br>(21,8)  |
| 84                  | 1.141<br>(28,99) | 1.165<br>(29,59) | 1.047<br>(26,6)  | 1.063<br>(27,0)  |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

PW (R-PDSO-G14)

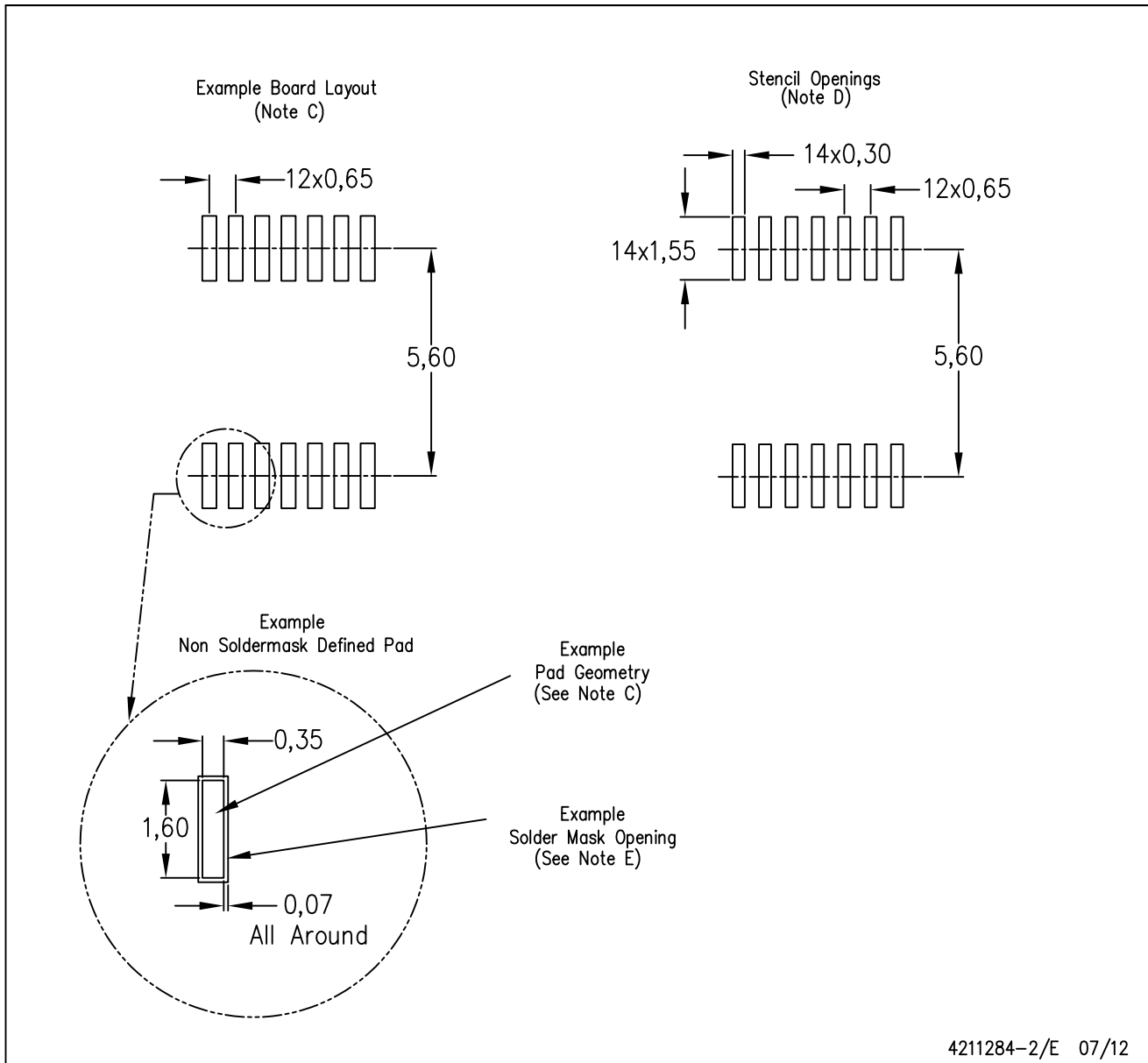
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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### Applications

|                               |  |
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