CD54HC4538, CD74HC4538, CD74HCT4538

High Speed CMOS Logic Dual Retriggerable Precision Monostable Multivibrator

Data sheet acquired from Harris Semiconductor
SCHS123

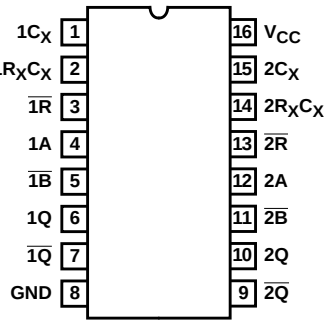
June 1998

Features

- **Retriggerable/Resettable Capability**
- **Trigger and Reset Propagation Delays Independent of R_X, C_X**
- **Triggering from the Leading or Trailing Edge**
- **Q and $\overline{Q}$ Buffered Outputs Available**
- **Separate Resets**
- **Wide Range of Output-Pulse Widths**
- **Schmitt Trigger Input on A and $\overline{B}$ Inputs**
- **Retrigger Time is Independent of C_X**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55°C to 125°C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}**

Pinout

CD54HC4538, CD74HC4538, CD74HCT4538
(PDIP, SOIC, CERDIP)
TOP VIEW



Description

The Harris CD54HC4538, CD74HC4538 and CD74HCT4538 are dual retriggerable/resettable monostable precision multivibrators for fixed voltage timing applications. An external resistor (R_X) and an external capacitor (C_X) control the timing and the accuracy for the circuit. Adjustment of R_X and C_X provides a wide range of output pulse widths from the Q and $\overline{Q}$ terminals. The propagation delay from trigger input-to-output transition and the propagation delay from reset input-to-output transition are independent of R_X and C_X.

Leading-edge triggering (A) and trailing edge triggering ($\overline{B}$) inputs are provided for triggering from either edge of the input pulse. An unused "A" input should be tied to GND and an unused $\overline{B}$ should be tied to V_{CC}. On power up the IC is reset. Unused resets and sections must be terminated. In normal operation the circuit retriggers on the application of each new trigger pulse. To operate in the non-triggerable mode $\overline{Q}$ is connected to $\overline{B}$ when leading edge triggering (A) is used or Q is connected to A when trailing edge triggering ($\overline{B}$) is used. The period (τ) can be calculated from $\tau = (0.7) R_X, C_X$; R_{MIN} is 5kΩ. C_{MIN} is 0pF.

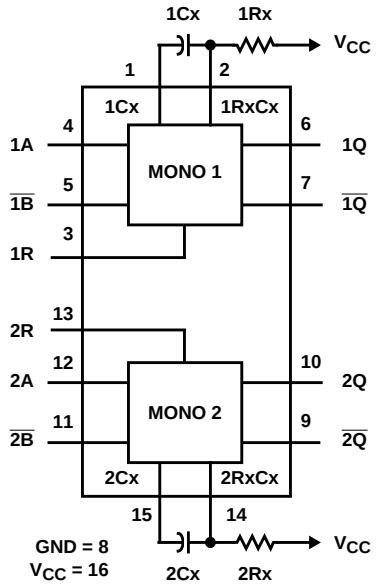
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD54HC4538F	-55 to 125	16 Ld CERDIP	F16.3
CD74HC4538E	-55 to 125	16 Ld PDIP	E16.3
CD74HCT4538E	-55 to 125	16 Ld PDIP	E16.3
CD74HC4538M	-55 to 125	16 Ld SOIC	M16.15
CD74HCT4538M	-55 to 125	16 Ld SOIC	M16.15

NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer and die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

Functional Diagram



TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{R}$	A	$\overline{B}$	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↓	⎍	⎍
H	↑	H	⎍	⎍

NOTE: H = High Level, L = Low Level, ↑ = Transition from Low to High, ↓ = Transition from High to Low, ⎍ One High Level Pulse, ⎍ One Low Level Pulse, X = Irrelevant.

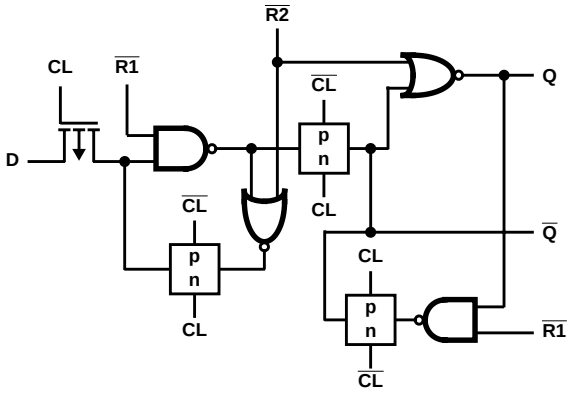


FIGURE 1. FF DETAIL

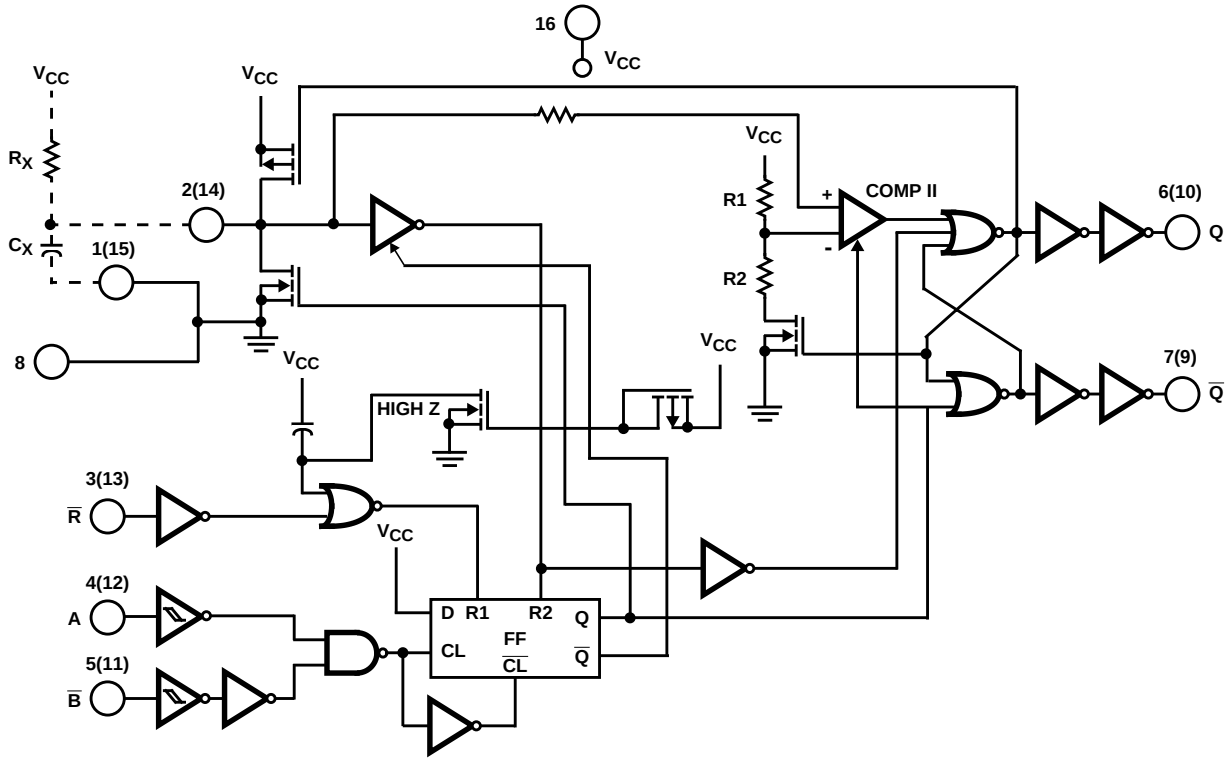


FIGURE 2. LOGIC DIAGRAM (1 MONO)

FUNCTIONAL TERMINAL CONNECTIONS

FUNCTION	V_{CC} TO TERMINAL NUMBER		GND TO TERMINAL NUMBER		INPUT PULSE TO TERMINAL NUMBER		OTHER CONNECTIONS	
	$MONO_1$	$MONO_2$	$MONO_1$	$MONO_2$	$MONO_1$	$MONO_2$	$MONO_1$	$MONO_2$
Leading-Edge Trigger/Retriggerable	3, 5	11, 13			4	12		
Leading-Edge Trigger/Non-Retriggerable	3	13			4	12	5-7	11-9
Trailing-Edge Trigger/Retriggerable	3	13	4	12	5	11		
Trailing-Edge Trigger/Non-Retriggerable	3	13			5	11	4-6	12-10

NOTES:

3. A retriggerable one-shot multivibrator has an output pulse width which is extended one full time period (T) after application of the last trigger pulse.
4. A non-triggerable one-shot multivibrator has a time period (T) referenced from the application of the first trigger pulse.

FIGURE 3. INPUT PULSE TRAIN

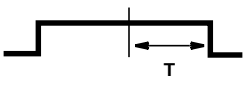


FIGURE 4. RETRIGGERABLE MODE PULSE WIDTH (A MODE)

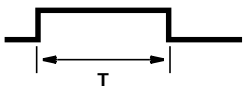


FIGURE 5. NON-RETRIGGERABLE MODE PULSE WIDTH (A MODE)

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . . -0.5V to 7V
DC Input Diode Current, I_{IK}
For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . . . ±20mA
DC Output Diode Current, I_{OK}
For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . . ±20mA
DC Output Source or Sink Current per Output Pin, I_O
For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . . ±25mA
DC V_{CC} or Ground Current, I_{CC} . . . . . ±50mA

Operating Conditions

Temperature Range, T_A . . . . . -55°C to 125°C
Supply Voltage Range, V_{CC} (Note 5)
HC Types . . . . . 2V to 6V
HCT Types . . . . . 4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O . . . . . 0V to V_{CC}
Input Rise and Fall Times, t_r, t_f
Reset Input:
2V . . . . . 1000ns (Max)
4.5V. . . . . 500ns (Max)
6V . . . . . 400ns (Max)
Trigger Inputs A or $\overline{B}$:
2V . . . . . Unlimited (Max)
4.5V. . . . . Unlimited (Max)
6V . . . . . Unlimited (Max)
External Timing Resistor, R_X (Note 6) . . . . . 5kΩ (Min)
External Timing Capacitor, C_X (Note 6) . . . . . 0 (Min)

Thermal Information

Thermal Resistance (Typical, Note 7)	θ_{JA} (°C/W)	θ_JC (°C/W)
PDIP Package	90	N/A
SOIC Package	160	N/A
CERDIP Package	130	55

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

5. Unless otherwise specified, all voltages are referenced to ground.
6. The maximum allowable values of R_X and C_X are a function of leakage of capacitor C_X, the leakage of the HC4538, and leakage due to board layout and surface resistance. Values of R_X and C_X should be chosen so that the maximum current into pin 2 or pin 14 is 30mA. Susceptibility to externally induced noise signals may occur for R_X > 1MΩ.
7. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS V_I (V)	TEST CONDITIONS I_O (mA)	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current A, $\overline{B}$, R	I_I	V_{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA
Input Leakage Current R_XC_X (Note 9)			-	6	-	-	±0.05	-	±0.5	-	±0.5	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	-	160	µA
Active Device Current Q = High & Pins 2, 14 at $V_{CC}/4$	I_{CC}	V_{CC} or GND	0	6	-	-	0.6	-	0.8	-	1	mA
HCT TYPES												
High Level Input Voltage	V_{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} and GND	-	5.5	-		±0.1	-	±1	-	±1	µA
Input Leakage Current R_XC_X (Note 9)			-	5.5	-	-	±0.05	-	±0.5	-	±0.5	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	5.5	-	-	8	-	80	-	160	µA
Active Device Current Q = High & Pins 2, 14 at $V_{CC}/4$	I_{CC}	V_{CC} or GND	0	5.5	-	-	0.6	-	0.8	-	1	mA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI_{CC} (Note 8)	V_{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	µA

NOTES:

8. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.
9. When testing I_{IL} the Q output must be high. If Q is low (device not triggered) the pull-up P device will be ON and the low resistance path from V_{DD} to the test pin will cause a current far exceeding the specification.

HCT Input Loading Table

INPUT	UNIT LOADS
All	0.5

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Table, e.g. 360µA max at 25°C.

Prerequisite for Switching Specifications

PARAMETER	SYMBOL	V_{CC} (V)	25°C			-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
HC TYPES												
Input Pulse Widths A, $\overline{B}$	t_{WH}, t_{WL}	2	80	-	-	100	-	-	120	-	-	ns
		4.5	16	-	-	20	-	-	24	-	-	ns
		6	14	-	-	17	-	-	20	-	-	ns
$\overline{R}$	t_{WL}	2	80	-	-	100	-	-	120	-	-	ns
		4.5	16	-	-	20	-	-	24	-	-	ns
		6	14	-	-	17	-	-	20	-	-	ns
Reset Recovery Time	t_{REC}	2	5	-	-	5	-	-	5	-	-	ns
		4.5	5	-	-	5	-	-	5	-	-	ns
		6	5	-	-	5	-	-	5	-	-	ns
Retrigger Time (Figure 11)	t_{rr}	5	-	175	-	-	-	-	-	-	-	ns
HCT TYPES												
Input Pulse Widths A, $\overline{B}$	t_{WH}, t_{WL}	4.5	16	-	-	20	-	-	24	-	-	ns
$\overline{R}$	t_{WL}	4.5	20	-	-	25	-	-	30	-	-	ns
Reset Recovery Time	t_{REC}	4.5	5	-	-	5	-	-	5	-	-	ns
Retrigger Time (Figure 11)	t_{rr}	5	-	175	-	-	-	-	-	-	-	ns

Switching Specifications C_L = 50pF, Input t_r, t_f = 6ns, R_X = 10KΩ, C_X = 0

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay A, $\overline{B}$ to Q	t_{PLH}	C_L = 50pF	2	-	-	250	-	315	-	375	ns
			4.5	-	-	50	-	63	-	75	ns
		C_L = 15pF	5	-	21	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	43	-	54	-	64	ns
A, $\overline{B}$ to $\overline{Q}$	t_{PHL}	C_L = 50pF	2	-	-	250	-	315	-	375	ns
			4.5	-	-	50	-	63	-	75	ns
		C_L = 15pF	5	-	21	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	43	-	54	-	64	ns
$\overline{R}$ to Q	t_{PHL}	C_L = 50pF	2	-	-	250	-	315	-	375	ns
			4.5	-	-	50	-	63	-	75	ns
		C_L = 15pF	5	-	21	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	43	-	54	-	64	ns
$\overline{R}$ to $\overline{Q}$	t_{PLH}	C_L = 50pF	2	-	-	250	-	315	-	375	ns
			4.5	-	-	50	-	63	-	75	ns
		C_L = 15pF	5	-	21	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	43	-	54	-	64	ns
Output Transition Time	t_{TLH}, t_{THL}	C_L = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Output Pulse Width R_X = 10k, C_X = 0.1µF	τ	C_L = 50pF	3	0.64	-	0.78	0.612	0.812	0.605	0.819	ms
			5	0.63	-	0.77	0.602	0.798	0.595	0.805	ms
Output Pulse Width Match, Same Package	-	-		-	±1	-	-	-	-	-	%
Power Dissipation Capacitance	C_{PD}	C_L = 15pF	5	-	136	-	-	-	-	-	pF
Input Capacitance	C_I	C_L = 50pF	-	10	-	10	-	10	-	10	pF
HCT TYPES											
Propagation Delay A, $\overline{B}$ to Q	t_{PLH}	C_L = 50pF	4.5	-	-	55	-	69	-	83	ns
		C_L = 15pF	5	-	23	-	-	-	-	-	ns
A, $\overline{B}$ to $\overline{Q}$	t_{PHL}	C_L = 50pF	4.5	-	-	55	-	69	-	83	ns
		C_L = 15pF	5	-	23	-	-	-	-	-	ns
$\overline{R}$ to Q	t_{PHL}	C_L = 50pF	4.5	-	-	40	-	50	-	60	ns
		C_L = 15pF	5	-	17	-	-	-	-	-	ns

Switching Specifications C_L = 50pF, Input t_r, t_f = 6ns, R_X = 10KΩ, C_X = 0 **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$\overline{R}$ to $\overline{Q}$	t_{PLH}	C_L = 50pF	4.5	-	-	50	-	63	-	75	ns
		C_L = 15pF	5	-	21	-	-	-	-	-	ns
Output Transition Time	t_{TLH}, t_{THL}	C_L = 50pF	4.5	-	-	15	-	19	-	22	ns
Output Pulse Width R_X = 10k, C_X = 0.1µF	τ	C_L = 50pF	5	0.63	-	0.77	0.602	0.798	0.595	0.805	ms
Output Pulse Width Match, Same Package	-	-	-	-	±1	-	-	-	-	-	%
Power Dissipation Capacitance	C_{PD}	C_L = 15pF	5	-	134	-	-	-	-	-	pF
Input Capacitance	C_I	C_L = 50pF	-	10	-	10	-	10	-	10	pF

NOTES:

10. C_{PD} is used to determine the dynamic power consumption, per one shot.

11. $P_D = (C_{PD} + C_X) V_{CC}^2 f_i \Sigma(C_L V_{CC}^2 f_O)$ where f_i = input frequency, f_O = output frequency, C_L = output load capacitance, C_X = external capacitance V_{CC} = supply voltage assuming $f_i \ll \frac{1}{\tau}$

Test Circuits and Waveforms

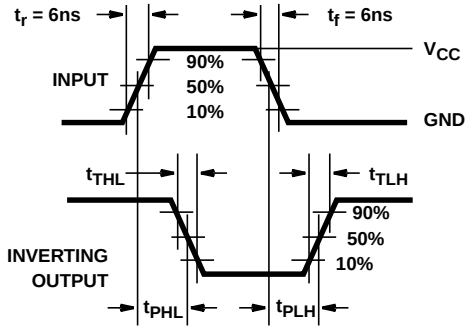


FIGURE 6. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

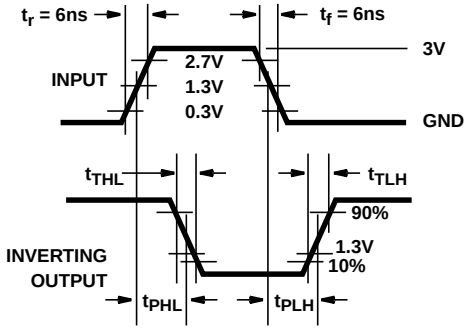


FIGURE 7. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

Typical Performance Curves

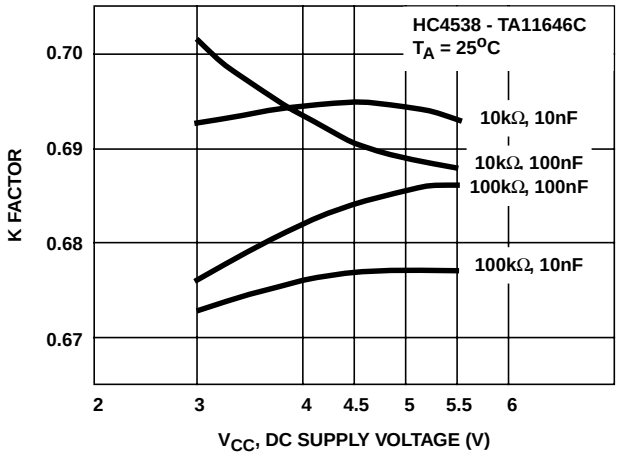


FIGURE 8. K FACTOR vs DC SUPPLY VOLTAGE (V_{CC}) - V

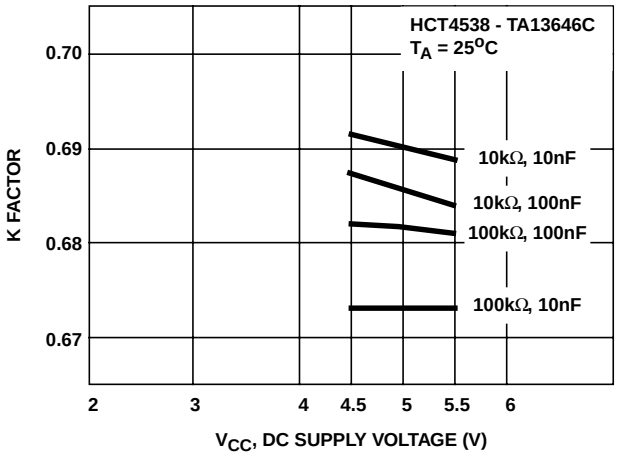


FIGURE 9. K FACTOR vs DC SUPPLY VOLTAGE (V_{CC}) - V

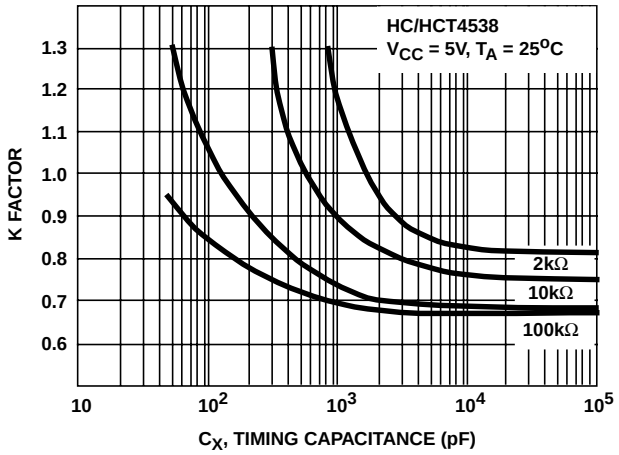


FIGURE 10. K FACTOR vs C_X

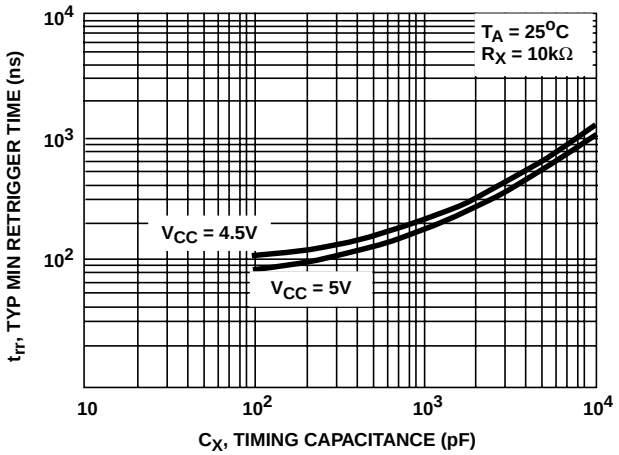


FIGURE 11. MINIMUM RETRIGGER TIME vs TIMING CAPACITANCE

Power-Down Mode

During a rapid power-down condition, as would occur with a power-supply short circuit with a poorly filtered power supply, the energy stored in C_X could discharge into Pin 2 or 14. To aviod possible device damage in this mode, when C_X is ≥ 0.5µF, a protection diode with a 1 ampere or higher rating (1N5395 or equivalent) and a separate ground return for C_X should be provided as shown in Figure 12.

An alternate protection method is shown in Figure 13, where a 51Ω current-limiting resistor is inserted in series with C_X. Note that a small pulse width decrease will occur however, and R_X must be appropriately increased to obtain the originally desired pulse width.

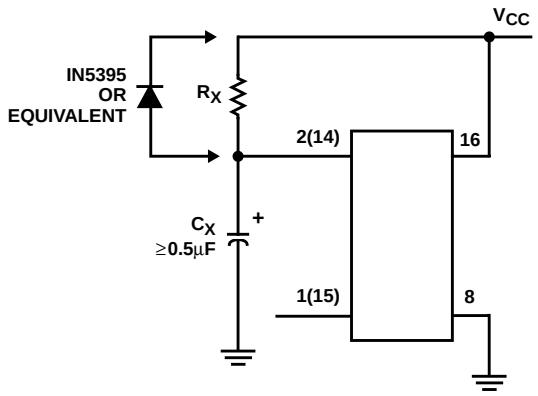


FIGURE 12. RAPID POWER-DOWN PROTECTION CIRCUIT

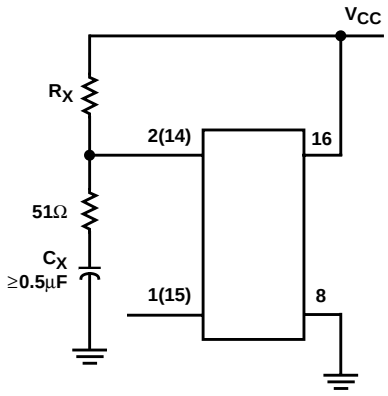


FIGURE 13. ALTERNATE RAPID POWER-DOWN PROTECTION CIRCUIT

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